AMENDMENT TO THE CLAIMS

Please **AMEND** claims 1, 7 and 10; and

Please **ADD** new claims 22-25 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

after the pFET stack is formed, providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

after the nFET stack is formed, providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel.

2. (Original) The method of claim 1, wherein the first layer of material is SiGe having a content of Ge approximately greater than 0% in ratio to Si.

3. (Original) The method of claim 1, wherein the second layer of material is Si:C.

4. (Original) The method of claim 3, wherein the Si:C has a content of C of about 4% or less.

5. (Previously Presented) The method of claim 1, wherein the first layer of material is unrelaxed SiGe and the second layer of material is unrelaxed Si:C and each of the first and second layers of material is formed at a thickness of between about 10 to 100 nm.

6. (Original) The method of claim 1, wherein:

the first layer of material is formed by placing a mask over the nFET channel and etching the regions of the pFET and selectively growing the first layer of material within the regions of the pFET channel; and

the second layer of material is formed by placing a mask over the pFET channel and etching regions of the nFET and selectively growing the second layer of material within the regions of the nFET channel.

7. (Currently Amended) ~~The method of claim 6, further comprising the steps of:~~ A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel;

the first layer of material being formed by placing a mask over the nFET channel and etching the regions of the pFET and selectively growing the first layer of material within the regions of the pFET channel, and the second layer of material being formed

by placing a mask over the pFET channel and etching regions of the nFET and selectively growing the second layer of material within the regions of the nFET channel;

providing a protection layer under the mask and over the nFET stack prior to the etching of the regions of the pFET stack and selectively growing the first layer of material; and

providing a protection layer under the mask and over the nFET stack prior to the etching of the regions of the pFET stack and selectively growing the second layer of material.

8. (Previously Presented) The method of claim 1, wherein the first layer of material and the second layer of material are each grown to a thickness about 10 to 100 nm.

9. (Original) The method of claim 1, wherein the first layer of material and the second layer of material are embedded in the layer.

10. (Currently Amended) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET structure and an nFET structure on the substrate associated with the pFET channel and the nFET channel, respectively; etching regions of the pFET structure and the nFET structure;

after the pFET stack is formed, forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel;

after the nFET stack is formed, forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel; and

doping source and drain regions of the nFET and pFET structures.

11. (Original) The method of claim 10, wherein the first material is SiGe and the second material is Si:C.

12. (Previously Presented) The method of claim 10, wherein:
the first material creates a compressive stress within the pFET channel; and
the second material creates a tensile stress within the nFET channel.

13. (Previously Presented) The method of claim 10, wherein:
the first material is formed by placing a protective layer over the nFET structure and the pFET structure and growing the first material within source and drain regions of the pFET channel; and
the second material is formed by placing a protective layer over the pFET structure and source and drain regions of the pFET structure and the nFET structure and growing the second material within source and drain regions of the nFET channel.

14. (Previously Presented) The method of claim 10, wherein the first material and the second material are embedded in the substrate.

15. (Previously Presented) The method of claim 10, wherein the first material and the second material are raised above a surface of the substrate.

16. (Previously Presented) The method of claim 10, wherein the first material and the second material each have a thickness of between about 10 to 100 nm.

17. (Original) The method of claim 10, wherein the first material is unrelaxed SiGe.

18. (Original) The method of claim 10, further comprising the step of in situ doping the first material with p-type doping and the second material with n-type doping to form the source and drain regions of the pFET and nFET, respectively.

Claims 19-21 (Canceled).

22. (New) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a pFET stack and an nFET stack on a substrate;

forming channels in the substrate about the pFET stack;

growing a layer of material in the channels associated with the pFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a compressive state within the channels of the pFET stack;

forming channels in the substrate about the nFET stack; and

growing a layer of material in the channels associated with the nFET stack, wherein after the growing, the layer of material has a lattice structure that tends to match a lattice structure of an underlying portion of the substrate to create a tensile state within the channels of the nFET stack.

23. (New) The method of claim 22, wherein:

before the layer of material in the channels associated with the pFET is grown, the layer of material has a lattice constant different than a base lattice constant of the substrate; and

before the layer of material in the channels associated with the nFET is grown, the layer of material has a lattice constant different than a base lattice constant of the substrate.

24. (New) The method of claim 22, wherein the channels about the pFET stack and the channels about nFET stack are formed by etching.

25. (New) The method of claim 22, wherein the channels about the pFET stack and the channels about the nFET comprise source/drain regions.